Advance Program

2016 International Symposium on

VLSI Technology, Systems and Applications

April 25-27, 2016

Ambassador Hotel Hsinchu, Taiwan

http://expo.itri.org.tw/2016vlsitsa

2016 VLSI-TSA Symposium Agenda (Tentative)

Time	Monday, April 25	
09:00 | 09:50	Ballroom A+B **Joint Opening & Award Ceremony**	
09:50 | 11:50	**J1: Joint Plenary Session** **09:50 J1-1: The present and future of Moore's law** Dr. Peng Bai, Intel Corporation **11:00 J1-2: New Systems Opportunities in Cloud-Scale Data Center** Dr. Tzi-Cker Chiueh, Industrial Technology Research Institute	
11:50 | 13:30	**Lunch**	
13:30 | 17:55	Ballroom A **T1: Special Session Foundry - the place where innovation turns to daily life products** **T3: Special Session Silicon Photonics** 15:35 Start	Ballroom C **T2: RRAM I** **T4: Novel Device I** 15:45 Start
18:30	**Cocktail Reception** (Ballroom B)	

Time	Tuesday, April 26		
08:30 | 10:10	Ballroom B **J2: Joint Plenary Session** **08:30 J2-1: "More than Moore" expands the Semiconductor World** Mr. Hidemi Takasu, ROHM Co., Ltd. **09:20 J2-2: More Than Moore's Law - Scaling with Silicon Photonics** Dr. Young-Kai Chen, Bell Laboratories, Nokia		
10:20 | 12:20	Ballroom A **T5: CMOS**	Ballroom B **T6: Special Session Advanced Memory Technologies**	Ballroom C **T7: 3D IC I**
12:20 | 13:30	**Lunch** 12:35-13:25 **Joint Luncheon Keynote** (Ballroom B)		
13:30 | 17:00	Ballroom A **T8: Processing Technologies** **T10: NVM** 15:50 Start	Ballroom B **J3: Special Session 5G/ IoT**	Ballroom C **T9: Novel Device II** **T11: 3D IC II** 16:00 Start
17:00 | 18:30		**Joint Panel Discussion**	

Time	Wednesday, April 27	
08:30 | 10:10	Ballroom B **J4: Joint Plenary Session** **08:30 J4-1: For Your Eyes Only? UAV and DJI** Prof. Zexiang Li, Hong Kong University of Science and Technology **09:20 J4-2: Taiwan 4G Progress and 5G Evolution** Mr. Mu-Piao Shih, Chunghwa Telecom Co., Ltd.	
10:20 | 12:25	Ballroom B **T12: Special Session Green Electronics**	Ballroom C **T13: RRAM II**
12:25 | 13:30	**Lunch**	
13:30 | 16:50	Ballroom A **TSA Short Course 1 Advanced Process Technology (ALD/ ALE)**	Ballroom B **TSA Short Course 2 Power Electronics**

The program is subject to change without prior notice.

CONFERENCE SCHEDULE

Joint Opening & Award Ceremony
Monday, April 25, 9:00 A.M. ~ 9:50 A.M.
Ballroom A+B

TSA General Chair and Co-chairs:	Carlos Mazure, Soitec, France C. T. Liu, Industrial Technology Research Institute, Taiwan
DAT General Co-chairs:	Donald Y.C. Lie, Texas Tech. University, USA Jiun-In Guo, National Chiao Tung University, Taiwan

2016 ERSO Award Recipients: TBD

2015 VLSI-TSA Best Student Paper Award Winners
Passivation of surface defects on InGaAs (001) and (110) surfaces in preparation for subsequent gate oxide ALD
Mary Edmonds, University of California San Diego, USA
Co-authors: T. J Kent, M. Chang, J.Kachian, R.Droopad, E. Chagarov, and A. C. Kummel
International Symposium on VLSI Technology, Systems and Applications, April 27-29, 2015
Digital Object Identifier: 10.1109/VLSI-TSA.2015.7117580
Publication Year: 2015

Ultrathin InAs-Channel MOSFETs on Si substrates
Cheng-Ying Huang, University of California, Santa Barbara, USA
Co-authors: Xinyu Bao, Zhiyuan Ye, Sanghoon Lee, Hanwei Chiang, Haoran Li, Varistha Chobpattana, Brian Thibeault, William Mitchell, Susanne Stemmer, Arthur Gossard, Errol Sanchez, and Mark Rodwell
International Symposium on VLSI Technology, Systems and Applications, April 27-29, 2015
Digital Object Identifier: 10.1109/VLSI-TSA.2015.7117566
Publication Year: 2015

2015 VLSI-DAT Best Paper Award Winners
A 127 fJ/conv. Continuous-Time Delta-Sigma Modulator with a DWA-Embedded Two-Step Time-Domain Quantizer, National Taiwan University, Taiwan
Co-authors: Chan-Hsiang Weng, Tzu-An Wei, and Tsung-Hsien Lin
International Symposium on VLSI Deign, Automation and Test, April 27-29, 2015
Digital Object Identifier:10.1109/VLSI-DAT.2015.7114517
Publication Year: 2015

Clock-Domain-Aware Test for Improving Pattern Compression, Mentor Graphics, USA
Co-authors: Kun-Han Tsai and Janusz Rajski
International Symposium on VLSI Deign, Automation and Test, April 27-29, 2015
Digital Object Identifier: 10.1109/VLSI-DAT.2015.7114506
Publication Year: 2015

Program Report

TSA Technical Program Chair and Co-chair:	Chorng-Ping Chang, Applied Materials, Inc., USA Chih-I Wu, Industrial Technology Research Institute, Taiwan
DAT Technical Program Co-chairs:	Wu Tung Cheng, Mentor Graphics, USA Jiun-Lang Huang, National Taiwan University, Taiwan

Session J1: Joint Plenary Session
Monday, April 25, 9:50 A.M. ~ 11:50 A.M.
Ballroom A+B
Co-chairs: Carlos Mazure, Soitec, France
Jiun-Lang Huang, National Taiwan University, Taiwan

9:50 A.M.

J1-1 The present and future of Moore's law

Peng Bai
Intel Corporation, USA

I will give an overview of industry leading and state of art Intel 14nm technology, present key results and enabling innovations, and highlight technology values for the products. I will briefly review the history of Moore's law, discuss challenges for continual silicon scaling, and describe important vectors in advancing Moore's law in the future.

10:40 A.M. Break

11:00 A.M.

J1-2 New Systems Opportunities in Cloud-Scale Data Center

Tzi-Cker Chiueh
Industrial Technology Research Institute, Taiwan

The world's ICT industries in the past decade have largely been driven by smartphones and various types of end user devices. As cloud-based applications and services become more and more prevalent, data centers that support these applications and services also present significant technical and commercial opportunities. In this talk, I will outline emerging technical requirements and trends in cloud data centers, and then elaborate on several new developments to illustrate exciting new opportunities in this area.

11:50 A.M. Lunch

Session T1: Special Session - Foundry - the place where innovation turns to daily life products (All Invited)
Monday, April 25, 1:30 P.M. ~ 3:15 P.M.
Ballroom A
Chair: Jean Pierre Raskin, Université Catholique de Louvain, Belgium

1:30 P.M.
T1-1 IMEC enables : technology services for emerging economies, startups, academia

Peter Lemmens
imec, Taiwan

Over the past 30 years, transistor technology has driven tremendous change in consumer, computer and communication industries. The next wave, internet of things, is massive and highly segmented, creating opportunities for many. Application Specific Integrated Circuits (ASICs) become more attractive due to significantly reduced costs and their ability to generate differentiation and IP protection. Many startups and large system houses, active in many different application domains, take advantage of this. They generate a new wave of hardware innovation, which we have labelled : substream innovation.
In this session we look at examples of such great companies bringing new and innovative products to market in many different IoT application domains.
We will illustrate how imec can help you, to turn your ideas into reality by providing access to world class research and inexpensive ASIC technology.

2:05 P.M.
T1-2 Foundry Solutions enabling next wave of SoC Innovations

Subramani Kengeri
GLOBALFOUNDRIES, USA

The rapid evolution of applications in the consumer and mobile space coupled with the emergence of the Internet of Things (IoT) are driving foundries to diversify design-technology solutions. This talk will discuss Foundry Solutions enabling next wave of SoC Innovations in power, performance, cost, and time-to-volume, while solving the issues of voltage scaling and integration of “user-experience” functions.

2:40 P.M.
T1-3 Foudnry Technology and Service

Jerry C. Hu
United Microelectronics Corporation, Taiwan

Future will be a smarter, greener, and ubiquitous connected world with proliferation of emerging applications like IoT. Integrating of Sensing, Security, Power Management, and Data Processing/Communication are getting important. With this market trend, we have observed larger volume and performance driven digital products follow Moore’s law, while analog intensive specialty applications, many offered by IDM, are migrating from 8” to 12” and from legacy to more advanced technologies. With this new market dynamics, foundry technology and service will also need to evolve to serve both large volume and growing fragmented markets. We believe foundry with comprehensive technology portfolio, collaborative ecosystem, and flexible business model, is essential to meet the growing demands.

3:15 P.M. Break

Session T2: RRAM I
Monday, April 25, 1:30 P.M. ~ 3:25 P.M.
Ballroom C
Co-chairs: SangBum Kim, IBM, USA
Shimeng Yu, Arizona State University, USA

1:30 P.M.

T2-1 ReRAM-based Analog Synapse and IMT Neuron Device for Neuromorphic System (Invited)

Kibong Moon, Euijun Cha, Daeseok Lee, Junwoo Jang, Jaesung Park, Hyunsang Hwang
POSTECH, South Korea

Although various new synapse devices were proposed, they could not meet the various requirements of ideal synapse devices for neuromorphic system. We developed analog synapse device using interface resistive switching characteristics by controlling the redox reaction at metal/conducting oxide interface. Compared with conventional filament RRAM which has intrinsic switching variability problems, interface switching device exhibits excellent switching uniformity and area scalability. By controlling the reactivity of metal and oxygen concentration in oxide film, we can modulate the resistance change characteristics under potentiation and depression conditions. By modulating the linearity and symmetry of conductance change, we have estimated the accuracy of pattern recognition. We found that synapse devices with linear and symmetric conductance change exhibit the best accuracy of pattern recognition.

2:05 P.M.

T2-2 Oxygen chemical potential profile optimization for fast low current (<10µA) resistive switching in Oxide-based RRAM

C.Y. Chen*, **, L. Goux*, A. Fantini*, A. Redolfi*, G. Groeseneken*, **, and M. Jurczak*
*imec, Belgium
**KU Leuven, Belgium

We explain in detail how to optimize the oxygen chemical potential profile of Ta_2O_5-based stack to improve switching speed at reduced operating current (<10µA). Using industry-relevant programming scheme, we demonstrate an oxide-based RRAM stack giving large on/off ratio (~x200) while the good reliability properties are preserved.

2:25 P.M.

T2-3 Excellent Resistance Variability Control of WOx ReRAM by a Smart Writing Algorithm

Yu-Hsuan Lin*, **, Jau-Yi Wu*, Ming-Hsiu Lee*, Tien-Yen Wang*, Yu-Yu Lin*, Feng-Ming Lee*, Dai-Ying Lee*, Erh-Kun Lai*, Kuang-Hao Chiang*, Hsiang-Lan Lung*, Kuang-Yeu Hsieh*, Tseung-Yuen Tseng**, and Chih-Yuan Lu*
*Macronix International Co., Ltd., Taiwan
**National Chiao Tung University, Taiwan

TMO ReRAMs, being built on defect states, are intrinsically subject to variability. In this work, cell to cell variability is studied by applying write shots with different current and voltage for Forming, SET and RESET operation, respectively. We found the keys to eliminate tail bits consist of (1) longer write pulse, (2) higher write current and (3) higher write voltage. In order to optimize the performance of write speed, write power and device reliability, we developed a novel resistance control method using a smart writing algorithm. Compared to the conventional ISPP writing scheme, this smart writing algorithm covers much wider switching condition variability and cell-to-cell variation by controlling both current and voltage for ReRAM operation.

2:45 P.M.

T2-4 Transient Control of Resistive Random Access Memory for High Speed and High Endurance Performance

Weijie Wang, Hongxin Yang, Victor Yiqian Zhuo, Minghua Li, Eng Keong Chua, and Yu Jiang
Data Storage Institute, A*STAR, Singapore

All advantages exhibited by RRAM devices are particularly striking for high density nonvolatile memory technology. However, 3D RRAM still suffer from poor endurance especially during high speed operation. We report the transient control method which enables a significant improvement of memory endurance. We demonstrated the stable transient control during fast pulse switching in different RRAM cell sizes of 1um~200nm. Endurance higher than 1xE7 cycles are achieved while keeping the ratio of high/low resistance level at 1xE3. Ultrafast switching with 1ns pulse width are demonstrated. We unveil the material switching dynamics responsible for stable transient processes, resulting in high RRAM endurance.

3:05 P.M.

T2-5 A Compact Model for the SET Parameter Variations of oxide RRAM Array

Lingjun Dai, Huaqiang Wu, Bin Gao, and He Qian
Tsinghua Univeristy, China

A physics-based compact model is developed to describe the parameter variations of oxide RRAM devices. The stochastic generation of oxygen vacancies and the variation of generation energy are considered in the model for the main reasons of the parameter fluctuation during SET process. The model is verified based on the measured data from 1kb 1T-1R RRAM array. Cycle-to-cycle variation and device-to-device variations of SET voltage and ON resistance are simulated by the model and compared with the experimental data. The model can be used for the simulation of large-scale memory arrays and logic or security circuits based on RRAM devices.

3:25 P.M. Break

Session T3: Special Session - Silicon Photonics (All Invited)
Monday, April 25, 3:35 P.M. ~ 5:20 P.M.
Ballroom A
Chair: Chee-Wee Liu, National Taiwan University, Taiwan

3:35 P.M.
T3-1 Industrialization of Silicon Photonics into a 300mm CMOS Fab
Kirk Ouellette
STMicroelectronics, Japan

Recently Silicon Photonics received a great deal of interest due to the increased need of high-data rate and low-cost transceivers in datacenters, mainly driven by cloud applications. In this paper we will demonstrate the industrialization of Si-Photonics in a CMOS fab addressing the datacenter market and more particularly the 100Gbits/s PSM-4 standard. We will discuss the co-integration scheme of electronics and photonics using 3D assembly and describe the photonics process flow and optical device performance. Finally we will discuss the future evolution of process development of the Silicon photonics.

4:10 P.M.
T3-2 Recent progress of 850nm VCSEL for oeic application
Hao-Chung Kuo
National Chiao Tung University, Taiwan

To meet the large demand of huge communication capacity, high-speed, energy-efficient light source provided by 850 nm vertical-cavity surface-emitting laser (VCSEL) are promising candidate, which shows superior ability in short reach optical links and interconnects. However, for the next generation communication systems like 5G mobile communication and 400 G Ethernet, current 850 nm VCSELs need significant improvement to meet higher data rate. In this report, the design and character of recent state-of-art high speed 850 nm VCSEL will be introduced.

4:45 P.M.
T3-3 Integrated Group IV Photodetectors via Rapid Melt Growth Method
Ming-Chang Lee
National Tsing Hua University, Taiwan

High-speed Group IV optoelectronics are nowadays a key technology platform for over 100Gbps data communication potentially applied in data centers, high-performance cluster computing, and cloud computing servers. However, unlike III-V compound semiconductors, all these Group-V devices are difficult to be monolithically integrated on the same substrate because of a large lattice mismatch between the elements. A process called rapid melt growth (RMG) method is applied to heterogeneously integrate monocrystalline Ge, Sn on Si substrate. This process doesn't require complex epitaxy process steps to deal with the lattice mismatch issue, and the thermal budget is low, which is potentially compatible with standard CMOS process. Several waveguide-based high-speed Si/Ge/Sn photodetectors are presented, including Si/Ge heterojunction waveguide pin, low-breakdown-voltage Si/Ge SAM avalanche photodiode and GeSn MSM photodetectors.

Session T4: Novel Device I
Monday, April 25, 3:45 P.M. ~ 5:55 P.M.
Ballroom C
Chair: Bing-Yue Tsui, National Chiao Tung University, Taiwan

3:45 P.M.
T4-1 Self Assembled Ordered Phthalocyanine Monolayers on 2D Semiconductors for Subnanometer dielectric ALD Nucleation (Invited)
Andrew C. Kummel
University of California, San Diego, USA

2-D materials for future semiconductor devices require ultrathin and defect-free dielectric layers as gate or channel insulators. However 2D semiconductors are un-reactive; thus, the dielectric layer selectively nucleates on defect sites or step edges creating large leakage current. In the present report, polar metal phthalocyanine molecules have been employed as an ALD template for high nucleation density deposition of dielectric layers. By combining in-situ scanning tunneling microscopy (STM) and fabrication graphene devices, the insulating property and growth mechanism of the dielectric layer have been elucidated.

4:20 P.M.
T4-2 Advanced Metrology and Inspection Solutions for a 3D World (Invited)
Ingo Schulmeyer*, Lorenz Lechner, Allen Gu, Raleigh Estrada, Diane Stewart, Lewis Stern, Shawn McVey, Bernhard Goetze, Ulrich Mantz, Raj Jammy
Carl Zeiss Microscopy GmbH, Germany/ USA

Semiconductor devices and packages have firmly moved in to an era where scaling is driven by 3D architectures. However, most of the metrology and inspection technologies in use today were developed for 2D devices and are inadequate to deal with 3D structures. An additional complication is the need for specific structural and defect information that may be buried deep within a 3D structure. We present concepts and technologies that allow for 3D imaging as well as tomography, enabling engineers to view structural information with unprecedented clarity, detail and speed.

4:55 P.M.
T4-3 P-type Surface Charge Transfer Doping of Black Phosphorus Field-effect Transistors
Yuchen Du, Lingming Yang, Hong Zhou, and Peide D. Ye
Purdue University, USA

In this work, a new approach to chemically dope black phosphorus (BP) is presented which significantly enhances device performance of few-layer BP field-effect transistors (FETs). By applying 2,3,5,6-tetrafluoro-7,7,8,8-tetracyanoquinodimethane (F4-TCNQ), low on-state resistance and high field-effect mobility are achieved, where the mobility has been increased from 181.1 cm^2/Vs to 228.5 cm^2/Vs and the on-state resistance has been decreased from 7.4 Ω·mm down to 3.2 Ω·mm, achieving a record high drain current of 531.8 mA/mm with a moderate channel length of 1.5 µm. In addition, transfer length method (TLM) structure has demonstrated a 2.9 times reduction in sheet resistance, and nearly 1.3 times decrease in contact resistance upon p-type surface charge transfer doping of BP FETs.

5:15 P.M.

T4-4 Performance Benchmarking of Monolayer and Bilayer Two-Dimensional Transition Metal Dichalcogenide (TMD) Based Logic Circuits

Chang-Hung Yu, Pin Su, and Ching-Te Chuang
National Chiao Tung University, Taiwan

For the first time, we have comprehensively evaluated and benchmarked the performance of logic circuits using monolayer and bilayer TMD devices based on ITRS 2028 node. Our study indicates that, with the excellent device electrostatics, the monolayer logic circuits exhibit comparable delay time and superior immunity to process variations, and thus favored for low-power applications; while the bilayer logic circuits are more suitable for relaxed channel length and high-performance applications.

5:35 P.M.

T4-5 Record high current density and low contact resistance in MoS_2 FETs by ion doping

Sara Fathipour, Hua-Min Li, Maja Remškar*, Lingyen Yeh**, Wilman Tsai**, Edward Chen**, Yuming Lin**, Susan Fullerton-Shirey***, and Alan Seabaugh
University of Notre Dame, USA
*Jožef Stefan Institute, Slovenia
**TSMC, Taiwan
***University of Pittsburgh, USA

Record high current density of 300 μA/μm with low contact resistance of 200 Ω μm and a channel length of 0.8 μm at a drain source bias of 1.6 V has been achieved for the first time in MoS_2 field-effect transistors (FETs) grown by chemical vapor transport. The low contact resistance is achieved using a polyethylene-oxide cesium-perchlorate solid polymer ion conductor formed by drop casting. The charged ions are placed into position over the channel by the application of a bias to a side gate and then locked into place by lowering the temperature.

Session J2: Joint Plenary Session
Tuesday, April 26, 8:30 A.M. ~ 10:10 A.M.
Ballroom B
Chair: Chorng-Ping Chang, Applied Materials, Inc., USA

8:30 A.M.

J2-1 "More than Moore " expands the Semiconductor World

Hidemi Takasu
ROHM Co., Ltd., Japan

The more Moore approach has been brought the remarkable progress to the semiconductor industry. However, this approach is getting difficult to produce excellent performance in comparison with the investment amount for it. Recently, the More than Moore approach is getting more interesting to enhance the value added and it's differentiation on semiconductor devices. New functions have been created on Si-LSI devices by applying new materials to Si-LSI technology. And new type of complex devices have been invented by merging plural different technology fields such as Bio-technology, Photonics, Micro mechanics, Electronics and etc. Here, CIGS film applied super high sensitive Image sensors, Ferro-electric film applied Non-Volatile logic devices, high efficient power modules used SiC devices, μ-TAS technology embedded Bio-sensors and more unique devices are presented.

9:20 A.M.

J2-2 More Than Moore's Law - Scaling with Silicon Photonics

Young-Kai Chen
Bell Laboratories, Nokia, USA

Rapid growth of intelligent mobile devices and internet of things demand instantaneous and ubiquitous access to large amount of data stored in remote data centers. This growth drives the need of very large capacity processors to store, switch and route vast amount of data. With the electronics industry embracing the "More-than-Moore" concept to increase the integration level of the data processors, future generations of CMOS technology must not only scale transistor dimensions, but also need to embrace various heterogeneous integration technologies with new processing architectures. The emerging silicon photonics technology, which is compatible with the main stream CMOS manufacturing processes, promises significant enhancement in processing speed and capacity. In this talk, we will review the current status of the silicon photonics technology and new capability it would enable.

10:10 A.M. Break

Session T5: CMOS
Tuesday, April 26, 10:20 A.M. ~ 12:20 P.M.
Ballroom A
Co-chairs: Shinichi Takagi, The University of Tokyo, Japan
Cheng-Tzung Tsai, United Microelectronics Corporation, Taiwan

10:20 A.M.

T5-1 SRAM cell performance analysis beyond 10-nm FinFET technology

Motoi Ichihashi, Youngtag Woo, and Sanjay Parihar
GLOBALFOUNDRIES, USA

This paper describes the performance analysis of SRAM cell capability beyond 10-nm FinFET technology. Through the circuit simulation with a pseudo memory macro, optimized SRAM cell can demonstrate almost the same performance of traditional metal architecture though the read-out delay analysis. Comparing between HD (High-Density) and HC (High-Current) cell, HD cell shows better performance in the large array macro due to the less parasitic resistance and capacitance.

10:40 A.M.

T5-2 Deep Understanding of Random Telegraph Noise (RTN) Effects on SRAM Stability

Dongyuan Mao, Shaofeng Guo, Ruheng Wang, Mulong Luo*, and Ru Huang
Peking University, China
* University of California, San Diego, USA

In this paper, multi-phonon transition model of RTN in FinFETs with statistical distribution is integrated into industry-standard BSIM-CMG, and read stability of SRAM is thoroughly examined. Different tendencies of SRAM failure probability plateau caused by RTN are found, which reflect real circuit operation situations. The impacts of RTN amplitude, bitline capacity, operation frequency on V_{min} are investigated in detail. Statistical results with impacts of RTN and process variations are also presented, which can be helpful for stability design and guard band prediction for SRAM.

11:00 A.M.

T5-3 Investigation of Local Heating Effect for 14nm Ge pFinFETs based on Monte Carlo Method

Longxiang Yin, Hai Jiang, Lei Shen, Juncheng Wang, Gang Du, and Xiaoyan Liu
Peking University, China

In this paper, we use 3D Full-band Ensemble Monte Carlo simulator and 3D Heat Conduction Equation Solver to investigate local heating effects in 14nm Ge pFinFETs. Statistical phonon spatial distribution is used as heating source. Size effects to thermal conductivity in nano-devices are considered. Phonon heating spatial distributions and several temperature distributions are demonstrated. The max temperature can be 591K and the degradation rate in output characteristics can be 19.6% at high gate and drain voltage. Max temperatures locations in different operation conditions are demonstrated. So, 14nm Ge pFinFETs will experience serious heat dissipation problems.

11:20 A.M.

T5-4 Corner Spacer Design for Performance Optimization of Multi-Gate InGaAs-OI FinFET with Gate-to-Source/Drain Underlap

Vita Pi-Ho Hu, Chang-Ting Lo*, Angada B. Sachid**, Pin Su*, and Chenming Hu**
National Central University, Taiwan
*National Chiao Tung University, Taiwan
**University of California, Berkeley, USA

Corner spacer design is investigated to improve the performance of multi-gate InGaAs-OI FinFET with gate-to-source/drain underlap compared with the all vacuum and all nitride spacer devices. All vacuum spacer devices with low permittivity reduce fringing capacitance and improve performance. However, for gate-to-source/drain underlap InGaAs-OI FinFET, all vacuum spacer device degrades Rsd and Ion, thus exhibiting slight improvement in inverter delay compared with the all nitride spacer device. Corner spacer design comprising of high-k and low-k composite spacer is proposed to optimize Rsd and capacitance, and hence improve delay. Various lengths and heights of corner spacer for InGaAs-OI FinFET with different underlap length and fin height aspect ratio are investigated to optimized performance. The optimized corner spacer design is: (a) the length of corner spacer is approximately equal to underlap length, and (b) the height of corner spacer is proportional to the sum of fin height and gate oxide thickness. Compared with the all vacuum spacer InGaAs-OI FinFET with Lun = 6 nm, the optimized corner spacer design exhibits 36% and 10% improvements in Ion and inverter delay, respectively.

11:40 A.M.

T5-5 Simulation of Nano-Scale Double Gate $In_{0.53}Ga_{0.47}As$ nMOSFETs by a Deterministic BTE Solver

Shaoyan Di*, Kai Zhao*,**, Zhiyuan Lun*, Tiao Lu*, Gang Du*, and Xiaoyan Liu*
*Peking University, China
**Beijing Information Science and Technology University, China

A nano-scale double gate $In_{0.53}Ga_{0.47}As$ nMOSFET device structure is simulated by deterministically solving the time dependent Boltzmann Transport Equation (BTE). The results show that the contribution of the L valleys cannot be ignored even if the energy gap between Γ and L valleys are very large. Moreover, the quasi-ballistic transport is observed despite the existence of scattering.

12:00 P.M.

T5-6 Optimization of Fin Profile and Implant in Bulk FinFET Technology (Late News Paper)

Y.-S. Wu, C.-H.Tsai, T. Miyashita, P.-N. Chen, B.-C. Hsu, P.-H. Wu, H.-H. Hsu, C.-Y. Chiang, H.-H. Liu, H.-L.Yang, K.-C Kwong, J.-C. Chiang, C.-W. Lee, Y.-J. Lin, C.-A. Lu, C.-Y. Lin, and S.-Y. Wu
TSMC, Taiwan

A comprehensive analysis of fin profile effect on bulk FinFET device characteristics is described in this paper. Optimal fin profile and anti-punch-through (APT) implant profile are important to DC performance and multiple-V_t offering capability, which are essential for system-on-chip (SoC) applications. This study provides practical device design guidelines for bulk FinFET technology.

12:20 P.M. Lunch

Session T6: Special Session - Advanced Memory Technologies (All Invited)
Tuesday, April 26, 10:20 A.M. ~ 12:05 P.M.
Ballroom B
Chair: Ming-Jinn Tsai, Industrial Technology Research Institute, Taiwan

10:20 A.M.

T6-1 A Novel Double-Density and Pitch Scalable Single-Gate Vertical-Channel (SGVC) 3D NAND Flash featuring a Flat-Channel Device

Hang-Ting Lue
Macronix International Co., Ltd., Taiwan

Different from the most often used gate-all-around (GAA) macaroni cell in 3D NAND Flash, we have developed a completely different flat-channel device with thin body for 3D NAND. The device is arranged in a SGVC architecture, where each single WL trench produces two physical bits directly, thus doubling the memory density by itself. The most important advantage of this flat cell is that it naturally has superior layer-to-layer uniformity even under non-ideal vertical etching, in sharp contrast to the GAA device. The device characteristics and array feasibility are discussed in this work.

10:55 A.M.

T6-2 Ultra-Low-Energy IOT Memory Architectures Based on Embedded STT-MRAM

Yu Lu
Hikstor Technology Co. Ltd, China

Emerging Internet-of-Things (IOT) demands an energy-efficient network of smart nodes. These devices need to be always-on, always-aware, and always-connected, despite the fact that their active duty cycles are low. Limited by intrinsic memory attributes, present IOT systems rely both on a nonvolatile storage and on a volatile working memory simultaneously. A unified memory subsystem, built on embedded STT-MRAM which can combine these two types of memories, can eliminate unnecessary energy-hungry transactions and improve the IOT energy efficiency dramatically. Furthermore, STT-MRAM can provide persistency, atomicity and anti-tearing for secure transactions, mitigating vulnerabilities of IOT devices.

11:30 A.M.

T6-3 Functionality and reliability of resistive RAM (RRAM) for non-volatile memory applications

Gabriel Molas
Cea Leti, France

Various RRAM concepts are currently being investigated (Oxide based RAM, Conductive Bridge RAM), all showing pros and cons depending on the architecture and memory stack.
As the specifications are strongly application-dependent, it is likely that the RRAM technology will be bound to a specific market segment. In this paper, we discuss the potential of RRAM for non-volatile memory applications, among them: storage class memory, embedded memory, programmable logic and neuromorphic applications.
By means of experimental studies and simulations, we analyze the role of the integrated materials on the memory performances and reliability and try to propose optimized stacks suitable for each targeted application.

12:05 P.M. Lunch

Session T7: 3D IC I

Tuesday, April 26, 10:20 A.M. ~ 12:15 P.M.
Ballroom C
Co-chairs: Ionut Radu, Soitec, France
Jia-Min Shieh, National Nano Device Laboratories, Taiwan

10:20 A.M.

T7-1 Key Enablers for 3D Sequential Integration (Invited)

Laurent Brunet
Cea Leti, France

3D sequential integrations such as CoolCube™ appear to be an alternative to planar scaling for the next generation nodes by stacking CMOS over CMOS and even transistors above transistors. This is possible thanks to high alignment accuracy depending only on the lithography stepper and not on the bonder performance, as in packaging technologies. Performance gain can be obtained either by optimizing each level independently or by the reduction in interconnect delay and thus, optimization of device partitioning and global routing. In this paper, data on the bottom transistors stability and some key enablers to realize a top transistor level at low temperature will be presented.

10:55 A.M.

T7-2 Implementation of Memory Stacking on Logic Controller by Using 3DIC 300mm Backside TSV Process Integration

Shang-Chun Chen, Pei-Jer Tzeng, Yu-Chen Hsin, Chung-Chih Wang, Po-Chih Chang, Jui-Chin Chen, Yiu-Hsiang Chang, Tsuen-Sung Chen, Tzu-Chien Hsu, Hsiang-Hung Chang, Chau-Jie Zhan, Chia-Hsin Lee, Yung-Fa Chou, Ding-Ming Kwai, Tzu-Kun Ku, Pei-Hua Wang, and We-Chung Lo
Industrial Technology Research Institute, Taiwan

Technologies of backside via-last TSV (BTSV) 3DIC 300mm process integration are developed to be applied in industry cooperation and mass production business model view. In this work, a successful BTSV process integration is disclosed and applied on 65nm logic controller/45nm DRAM stacking structure. Key enabling process technologies in BTSV formation and thin wafer handling are discussed. The electrical measurement data and functional logic circuit test show the practicability of BTSV integration.

11:15 A.M.

T7-3 Impact of Transistor Technology on Power Savings in Monolithic 3D ICs

Sandeep Kumar Samal*,**, Deepak Kumar Nayak*, Motoi Ichihashi*, Srinivasa Banna*, and Sung Kyu Lim**
*GLOBALFOUNDRIES, USA
**Georgia Institute of Technology, USA

In this paper, we discuss the impact of transistor technology on the power savings in monolithic 3D ICs over traditional 2D ICs. Our results are based on gate-level 3D IC partitioning and full RTL to GDSII design and analysis of a Low Density Parity Check (LDPC) benchmark circuit block with use of two different silicon validated foundry technologies. These two technologies have the same nominal operating voltage, but differ in terms of device performance, power, and gate capacitance. Our results show that monolithic 3D IC provides 37.5% more power savings for the technology with lower device power and input capacitance compared to that of a high power device technology.

11:35 A.M.

T7-4 A-SiGeC Thin Film Photovoltaic Enabled Self-Power Monolithic 3D IC Under Indoor Illumination

Ming-Hsuan Kao*, Chih-Chao Yang**, Tsung-Ta Wu**, Tung-Ying Hsieh**, Wen-Hsien Huang**, Hsing-Hsiang Wang**, Chang-Hong Shen**, Wen-Kuan Yeh**, Meng-Fan Chang***, and Jia-Min Shieh*,**
*National Chiao Tung University, Taiwan
**National Nano Device Laboratories, Taiwan
***National Tsing Hua University, Taiwan

Low temperature a-SiGeC thin film photovoltaic (TFPV) ambient light-energy harvesters monolithically integrated with high performance 3D sequentially stackable device were demonstrated in this article. The 3D stackable device with threshold voltage engineering and driving current boosting technologies enable excellent current controllability to achieve low I_{off} and high I_{on} operation condition for integrated circuit design. The monolithically stacking of Si thin-film energy harvester, which provide output power (21.93uW/cm^2) under 450 lux indoor illumination, envisions self-power and low cost 3D$^+$IC for internet of things.

11:55 A.M.

T7-5 Reliable High-Voltage Amorphous InGaZnO TFT for Monolithic 3D Integration

Ming-Jiue Yu, Ruei-Ping Lin, Yu-Hong Chang, and Tuo-Hung Hou
National Chiao Tung University, Taiwan

The wide band-gap a-IGZO is a promising channel material to realize high-voltage transistors that can be easily integrated on logic ICs by low-temperature 3D stacking. This monolithic 3D integration would enable on-chip power management to improve power consumption and integration density. We report a high-voltage a-IGZO TFT with the high-k Al_2O_3 gate dielectric. By using a low-temperature process below 200 ^oC, excellent transistor characteristics, including a current on/off ratio of 10^9, steep subthreshold swing of 0.1 V/decade, high breakdown voltage of 45 V, and robust bias stress reliability have been demonstrated.

12:15 P.M. Lunch

Joint Luncheon Keynote
Tuesday, April 26, 12:35 P.M. ~1:25 P.M.
Ballroom B
Chair: Raj Jammy, Carl Zeiss, USA

Genomics and Personalized Medicine of the Future

Bharath Takulapalli
Founder & CEO
INanoBio, USA

Genome profiling is revolutionizing cancer therapy by empowering the physician and enabling precision medicine. The standard of care is rapidly shifting to individualized medicine based on genetic profile of disease in a patient. Towards this, at INanoBio we are developing an advanced $100 high-accuracy whole genome sequencer. We believe that genomics based diagnostics, genomic medicine and gene therapy are going to transform all areas of healthcare, propelling us towards an almost disease-free society in about 25 years, where 75% of current diseases can be diagnosed early and simply preempted.

Session T8: Processing Technologies
Tuesday, April 26, 1:30 P.M. ~ 3:30 P.M.
Ballroom A
Chair: Robert D. Clark, TEL Technology Center, America, LLC, USA

1:30 P.M.

T8-1 Low Contact Resistivity (1.5×10^{-8} Ω-cm^2) of Phosphorus-doped Ge by In-situ Chemical Vapor Deposition Doping and Laser Annealing

S. -H. Huang*, F. -L. Lu*, and C. W. Liu*, **
*National Taiwan University, Taiwan
** National Nano Device Laboratories, Taiwan

The electron concentration of 3×10^{20} cm^{-3} in phosphorus-doped Ge is obtained by in-situ chemical vapor deposition doping and laser annealing. The laser annealing effectively improve the crystallinity in the Ge layer. The pulse laser not only activates the phosphorus, but also produces the biaxial tensile strain. With the nickel germanide contact, the contact resistivity is as low as 1.5×10^{-8} Ω-cm^2 by greatly reducing the tunneling distance. The misfit dislocations at the Ge/Si interface lead to the ideality factor of 1.6 for the Ge/Si hetero-junction diode with on/off ratio of $\sim 1\times10^5$.

1:50 P.M.

T8-2 Low Temperature Microwave Annealed FinFETs with Less Vth Variability

K. Endo, Y. -J Lee*, Y. Ishikawa, F. -K. Hsueh*, P. -J. Sung*, Y. -X. Liu, T. Matsukawa, S. O'uchi, J. Tsukada, H. Yamauchi, and M. Masahara
National Institute of Advanced Industrial Science and Technology, Japan
* National Nano Device Laboratories, Taiwan

FinFETs with the low temperature microwave annealing process have been successfully fabricated and the superiority of the microwave annealing process has been precisely studied. For the first time, it is revealed that the microwave annealed FinFET exhibits less Vth variability and lower gate leakage.

2:10 P.M.

T8-3 $In_{0.53}Ga_{0.47}As$(001)-(2x4) and $Si_{0.5}Ge_{0.5}$(110) surface passivation by self-limiting deposition of silicon containing control layers

M. Edmonds, T. J. Kent, S. Wolf, K. Sardashti, M. Chang*, J. Kachian*, R. Droopad**, E. Chagarov, and A. C. Kummel
University of California, San Diego, USA
*Applied Materials, USA
**Texas State University, USA

Si-H_x, and Si-OH seed layers were deposited on InGaAs(001)-(2x4) via two separate self-limiting CVD processes, and an Si-N_x seed layer was deposited on $Si_{0.5}Ge_{0.5}$ (110) via an ALD process. XPS in combination with STS/STM were employed to characterize the electrical and surface properties of these silicon containing control layers on InGaAs(001)-(2x4) and $Si_{0.5}Ge_{0.5}$ (110) surfaces. MOSCAP device fabrication was performed on n-type InGaAs(001) substrates with and without a Si-H_x passivation control layer deposited by self-limiting CVD in order to determine the effects on C_{max}, frequency dispersion, and midgap trap states.

2:30 P.M.

T8-4 Electrical Defect Spectroscopy and Reliability Prediction Through a Novel Simulation-Based Methodology

L. Larcher*,**, G. Sereni*, A. Padovani*,**, and L. Vandelli*,**
*University of Modena and Reggio Emilia, Italy
**MDLab s.r.l., Italy

The semiconductor technology development requires a full understanding of material implications at the device level. This requires connecting the microscopic/atomic properties of the material (e.g. defect) to the macroscopic electrical characteristics of the device. In this scenario, we developed a new methodology, supported by a multi-scale modeling and simulation (MS) software [1], [2], which allows extracting from the simulations of the electrical characterization measurements (I-V, C-V, G-V, BTI, Charge-Pumping, noise, stress) the material and device properties that can be used for the technology development, the design of novel devices and the analysis of the device reliability also at statistical level (TDDB, leakage currents).

2:50 P.M.

T8-5 RF Performance of Passive Components on State-of-Art Trap Rich Silicon- on-Insulator Substrates

Lei Zhu*,**, Shuangke Liu*, F. Allibert***, E. Desbonnets***, I. Radu***, Xinen Zhu* and Yumin Lu*,**
*Shanghai Industrial µTechnology Research Institute, China
**Shanghai Institute of Microsystem and Information Technology, China
***SOITEC, France

Trap rich silicon-on-insulator (TR-SOI) substrates have been widely adopted for high performance RFICs in cellular front-ends over the past few years. With the more stringent loss and harmonic requirements for 4G and even 5G networks, TR-SOI substrate's quality has been improved continuously since its introduction. Two representative types of commercially available TR-SOI substrates are investigated in this paper to demonstrate both small and large signal performance up to 10 GHz. 50 Ohm CPW lines and spiral inductors were fabricated on HR-SOI, TR-SOI, and quartz substrates. The experiment results show that TR-SOI substrates present attenuation coefficient less than 0.2 dB/mm, which is close to that of quartz substrates, and much improved harmonic suppression than HR-SOI substrates.

3:10 P.M.

T8-6 PMOS Contact Resistance Solution Compatible to CMOS Integration for 7 nm Node And Beyond (Late News Paper)

C.-N. Ni, Y.-C. Huang, S. Jun, S. Sun, A. Vyas, F. Khaja, K.V. Rao, S. Sharma, N. Breil, M. Jin, C. Lazik, A. Mayur, J. Gelatos, H. Chung, R. Hung, M. Chudzik, N. Yoshida, and N. Kim
Applied Materials, USA

We report a PMOS contact resistivity (ρc) improvement strategy by forming Ge-rich contact interface which is compatible to Ti/Si(Ge) system and CMOS integration flow. Short pulsed (nsec) laser anneal and advanced treatment during pre-clean have shown to be effective to segregate Ge towards SiGe surface resulting in PMOS ρc improvement. With Ge% increasing from 45 to 100%, ρc improved three-fold, from $1.2e^{-8}$ to $2.8e^{-9}$ Ωcm^2, due to bandgap modulation and preferred Fermi-level pinning. In the end, we propose a CMOS-integration-compatible contact flow which addresses ρc optimization for both PMOS and NMOS contact.

3:30 P.M. Break

Session J3: Special Session - 5G/ IoT (All Invited)
Tuesday, April 26, 1:30 P.M. ~ 4:45 P.M.
Ballroom B
Co-chairs: Franz Dielacher, Infineon Technologies Austria AG, Austria
Donald Y.C. Lie, Texas Tech. University, USA

1:30 P.M.
J3-1 Trend, Technology and Architecture of Small Cell in 5G Era
Chun-Nan Liu
Industrial Technology Research Institute, Taiwan

With the mobile data traffic increasing, network operators are urgently looking for new technologies for improving capacity, user data-rates, spectrum reuse and latency to fulfill user experience and variant new applications. Small cells will play an important role in the high capacity, densely deployed networks for future 5G networks. The small cells in 5G will address on carrier aggregation, licensed and un-licensed band, mmWave, new waveform/coding/modulation, multi-cell cooperation and advanced MIMO technologies, etc. for the three 5G major use cases: Enhanced Mobile Broadband, Massive Machine Type Communications and Ultra-reliable and Low Latency Communications.

2:05 P.M.
J3-2 Doherty technique for 5G RF and mm-wave Power Amplifiers
Patrick Reynaert
KU Leuven, Belgium

The 5G requirements are for sure challenging for designing an RF or mm-wave power amplifier in CMOS or SOI. This talk will focus on some of these challenges and will then discuss the Doherty technique as a way to implement PAs with high bandwidth, efficiency and linearity. The Doherty architecture will be compared with other architectures such as outphasing, polar modulation and envelope tracking. Finally, several examples will be discussed in more detail to explain the design procedures of such 5G PAs in CMOS and SOI.

2:40 P.M.
J3-3 Mixed Analog-Digital Pulse-Width Modulator for Massive-MIMO Transmitters
Yannis Papananos, Nikolaos Alexiou, Konstantinos Galanopoulos, David Seebacher, and Franz Dielacher
Infineon Technologies Austria AG, Austria

This paper presents a mixed-signal outphasing RF-PWM modulator with improved time resolution and high dynamic range realized in 40nm CMOS. Phase shifting is implemented using synchronously tapped analog delay lines comprising integrated L and C devices and achieving a fine-step delay of 2 ps while occupying acceptable silicon area and consuming zero power. The analog outputs of the delay lines is converted to CMOS-compatible square pulses that drive an AND gate which generates RF-PWM pulses with minimum pulse width of 10ps on a 50-Ohm load. According to system-integrated modulator co-simulation results, an ACLR of -45dBc is achieved from a 40 MHz baseband signal on a 2.65 GHz carrier.

3:15 P.M. Break

3:35 P.M.

J3-4 Ultra-low Power SoC for Wearable & IoT

Uming Ko
MediaTek, USA

With the landmark introduction of Smartphone in 2007, Mobile Internet and computing took off and the associated data bandwidth continue to grow exponentially. To satisfy the ever-increasing computing requirements, mobile CPU clock frequencies have exceeded GHz. However, the technology will soon hit a frequency wall beyond which cost becomes prohibitively high. Thus, mobile clients are rapidly moving to multi-core CPU and GPU to enable consumer applications and mobile human-interface devices (HIDs), with system-adaptive power management, thermal throttling, and heterogeneous multi-processing, for optimal performance and energy efficiency within thermal limits. The insatiable computation need, coupled with the explosion of Internet-of-Things (IoT) and wearable devices for long battery operation will continue to driver the IC technology forward. But, with the constraints of portable-device form factors and limited battery-technology improvement, the energy and thermal gaps present major technical challenges. To overcome these challenges, many innovations are desperately needed to enable the ubiquitous ecosystem that promises to provide ample possibilities to enhance and enrich everyone's life.

4:10 P.M.

J3-5 5G and IoT

Li Fung Chang
Industrial Technology Research Institute, Taiwan

As vision and service requirements for 5G have converged in the cellular industry. Three service types are identified: enhanced Mobile BroadBand (eMBB), enhanced Machine Type Communication (eMTC), and uMTC (ultra-reliable, ultra-low latency MTC). The latter two are more related to IoT with different flavors compared to the existing IoT services. In this talk, I will discuss the enabling technologies and challenges in 5G and provide an update on the 3GPP standard development in cellular IoT.

4:45 P.M. Break

Session T9: Novel Device II
Tuesday, April 26, 1:30 P.M. ~ 3:45 P.M.
Ballroom C
Co-chairs: Peide Ye, Purdue University, USA
Hiroyuki OTA, National Institute of Advanced Industrial Science and Technology, Japan

1:30 P.M.

T9-1 The Opportunity for bulk GaN Power Device - Technology and Application (Invited)

Zhen-Yu Li
HUGA OPTOTECH INC., Taiwan

GaN-based wide band-gap semiconductors have attracted much attention due to their excellent properties, such as high breakdown electric field, high power switching efficiency and high thermal stability. Besides, the inherent polarization is built in AlGaN/GaN hetero-junction structure, and further promises higher sheet carrier density (ns) in the two dimensional electron gas (2DEG), as well as a diminution of on-state resistance (Ron) for power switching applications. In particular, the loss at high frequency (about 1MHz) was lower than Si device by a factor of 10. It's means that high frequency operation is a strong probability for GaN device. In other words, the system size and weight can be reduced drastically by using GaN device because of smaller filter and less passives. Nevertheless, there is still lack of suitable substrates for GaN-based devices to develop fully their superiorities. In recent decades, many studies of the growth of GaN-based epilayers on a variety of substrates, such as sapphire, SiC, bulk GaN, and Si, had been published. Among the aforementioned substrate materials, bulk GaN is regarded as a relatively promising substrate for use in GaN-based epitaxy due to homo-epitaxial growth. It was well-known that the largest obstacle for the development of GaN-on-GaN power device is the substrate. Typically, free-standing GaN substrate today are fabricated by hydride vapor phase epitaxy (HVPE) using MOCVD-grown GaN-on-sapphire template. However, the threading dislocation densities (TDDs) are still ranging from $3x10^6$–$1x10^7$ cm^{-2}. On the other hand, many papers pointed out that leakage would be easily occurred from channel to substrate through threading dislocations (TDs), accelerate degradation of GaN power device, and have a well-documented negative impact on GaN power device lifetime. Consequently, TDDs below 10^4 cm^{-2}, as are available in GaAs and should be available in true bulk GaN, are often regarded as being necessary for vertical GaN-on-GaN power devices.

2:05 P.M.

T9-2 Short-Channel BEOL ZnON Thin-Film Transistors with Superior Mobility Performance

Chin-I Kuan, Horng-Chih Lin, Pei-Wen Li, and Tiao-Yuan Huang
National Chiao Tung University, Taiwan

This work reports the first experimental submicron and sub-100 nm ZnON TFTs with excellent performance. Field-effect mobility values as high as 55 and 9.2 cm^2/V-s were measured from ZnON TFTs with channel lengths of 0.5 µm and 75 nm, respectively. Those are the highest values ever reported on oxide-semiconductor TFTs of comparable channel length. The results confirm ZnON TFTs as an effective building block for the construction of BEOL circuits integrated in a chip.

2:25 P.M.

T9-3 High-gain, Low-voltage BEOL Logic Gate Inverter Built with Film Profile Engineered IGZO Transistors

Rong-Jhe Lyu, Yun-Hsuan Chiu, Horng-Chih Lin, Pei-Wen Li, and Tiao-Yuan Huang
National Chiao Tung University, Taiwan

We demonstrate InGaZnO (IGZO) TFTs with channel-length (L) tunable V_{th} for high-gain BEOL logic gate inverters in a unique film-profile engineering (FPE) approach. In this FPE scheme the thickness and film profile of gate oxide and IGZO active layer are directly tailored by L (0.4—0.8 μm) in a single step, leading to a wide-ranging tunability in V_{th} of -0.2—+1.6V at no expense of additional masks and process steps. This provides an effective degree of freedom in the layout design for the realization of area-saving, high-gain unipolar logic inverters with load-transistors. Record-high voltage gain of 112 is demonstrated from the unipolar logic inverter with depletion-load 0.4 μm IGZO TFT and 0.7 μm IGZO drive-transistor, respectively, at operation voltage (V_{DD}) of 9V.

2:45 P.M.

T9-4 Nickel-Phosphide Contact for Effective Schottky Barrier Modulation in Black Phosphorus P-Channel Transistors

Zhi-Peng Ling, Kausik Majumdar*, Soumya Sakar, Sinu Mathew, Jun-Tao Zhu, K. Gopinadhan, T. Venkatesan, and Kah-Wee Ang
National University of Singapore, Singapore
*Indian Institute of Science, India

We demonstrate a new contact technology for realizing a near band edge contact Schottky barrier height (Φ_B) in black phosphorus (BP) p-channel transistors. This is achieved via the use of high work function nickel (Ni) and thermal anneal to produce a novel nickel-phosphide (Ni_2P) alloy which enables a record low hole Φ_B of ~12 meV. The formation of reactive Ni_2P/BP contact was found to further improve the transmission probability as compared to the Ni/BP contact. Moreover, the penetration of Ni_2P in the source and drain regions could additionally reduce the parasitic series resistance, leading to drive current improvement.

3:05 P.M.

T9-5 Experimental Demonstration of Performance Improvement with a Strain Boost Technique Tailored for 3-Dimensional Structure on Nano-Scaled Bulk *p*FinFETs

Ta-Chun Lin, Yun-Ju Sun, Ming-Huei Lin, Tomonari Yamamoto, and Shyh-Horng Yang
Taiwan Semiconductor Manufacturing Company, Taiwan

We demonstrated a strain boost technique tailored for 3-Dimensional (3-D) structure on *p*FinFETs so the longitudinal stress can be locally maximized in the fin. The resulting effective mobility improvement by this technique was effectively transferred to the enhancement of the injection velocity. The saturation drain current and the ring oscillator speed under the same electrostatics were hence improved by 5% and 3% at V_{dd}=0.8V, respectively. Moreover, the electrical characteristics at the varied V_{dd} and temperatures, the fin number dependence, and the local variability were also systematically discussed in this paper.

3:25 P.M.

T9-6 Fine charge sensing using a Silicon Nanowire for Biodetection

Corentin Carmignani, Olivier Rozeau, Pascal Scheiblin, Aurélie Thuaire, Patrick Reynaud, Sylvain Barraud, Thomas Ernst, Severine Cheramy, and Maud Vinet
Cea Leti, France

This paper proposes an extensive analysis of the impact of both structural effect and charge parameters on silicon nanowire-based biological sensors, for single-charge detection. These parameters are calibrated on physical and electrical characterizations and are subsequently introduced in a compact model to predict the signal over noise ratio (SNR). We finally propose rules for the design of nanowires and recommendations for the placement of the biological element, inducing the single charge release.

3:45 P.M. Break

Session T10: NVM
Tuesday, April 26, 3:50 P.M. ~ 4:50 P.M.
Ballroom A
Chair: Jau-Yi Wu, Macronix International Co., Ltd., Taiwan

3:50 P.M.
T10-1 A TiO_2-based Volatile Threshold Switching Selector Device with 10^7 non linearity and sub 100pA off current
Simone Cortese, Maria Trapatseli, Ali Khiat, and Themistoklis Prodromakis
University of Southampton, United Kingdom

ReRAM crossbar arrays are known to be susceptible to the presence of the sneak current issue during the readout operations which undermines crossbar scaling. This problem can be solved by the addition of an highly non-linear two-terminal selector device. In this work we present a 5 nm thick TiO_2-based selector which exploits a volatile threshold resistive switching, so far unreported for this material. The device shows a current density up to 100 kA/cm^2, 10^7 current non-linearity and a 4 V voltage margin, the highest reported for TiO_2-based selectors and sub 100 pA off current.

4:10 P.M.
T10-2 Variable-length Gateless Transistor for Analog One-Time-Programmable Memory Applications
Po-Ruei Cheng, Chih-Sung Yang, Meng-Yin Hsu, Chrong Jung Lin, and Ya-Chin King
National Tsing-Hua University, Taiwan

This work presents a novel embedded Analog Gateless One-Time-Programming Memory (AG-OTP), implemented by standard CMOS logic process. The NVM cell includes a gateless storage node in series with a select transistor; where the charge stored on the parasitic ONO structure. The p-channel device is programmed by channel hot hole induced hot electron injection (CHHIHE). An angled-shaped source region allows the gateless channel to be partially turned-on and gradually increase the read current level. This unique structure enable the storage of analog data as continuous read current can be readily achieved.

4:30 P.M.
T10-3 An Innovative 1T1R Dipole Dynamic Random Access Memory (DiRAM) featuring High Speed, Ultra-low power, and Low Voltage Operation
E. R. Hsieh, C. H. Chuang, and Steve S. Chung
National Chiao Tung University, Taiwan

For the first time, a new 1T1R of volatile memory based on the interfacial dipole flipping mechanism, named as Dipole Dynamic Random Access Memory (DiRAM), has been reported. It features 4ns per bit of dipole switching time, larger than 10^9 of endurance, and 10 seconds of retention with reasonable positive and negative resistance window, low operation voltages with bit line at 0.8V and word line at 0.2V, and around 1 nano-Watt per bit of operation power. DiRAM is also easy to be integrated with state-of-the-art CMOS technology. The results have shown that this volatile memory may be a potential candidate for the next generation DRAM technology.

4:50 P.M. Break

Session T11: 3D IC II
Tuesday, April 26, 4:00 P.M. ~ 5:00 P.M.
Ballroom C
Chair: Chih-Lin Wang, Industrial Technology Research Institute, Taiwan

4:00 P.M.
T11-1 Wafer-Level MOSFET with Submicron Photolysis Polymer Temporary Bonding Technology Using Ultra-Fast Laser Ablation for 3DIC Application

Chuan-An Cheng, Yu-Hsiang Huang, Chien-Hung Lin*, Chia-Lin Lee*, Shan-Chun Yang*, and Kuan-Neng Chen
National Chiao Tung University, Taiwan
*Kingyoup Optronics Co., Ltd, Taiwan

A submicron photolysis polymer temporary bonding with ultra-fast laser de-bonding process of less than 20 s has been demonstrated where both photolysis polymer and polyimide are served as release layer and adhesive layer, respectively. In addition, the bonded structure provides high chemical resistance and mechanical strength for handling process. By measuring the electrical characteristics of devices before and after de-bond, it shows promising performance without degradation. Thus it can be a potential candidate for temporary bonding and de-bonding in 3D integration.

4:20 P.M.
T11-2 Compact Modeling and Simulation of TSV with Experimental Verification

Jhih-Yang Yan, Sun-Rong Jan, Yi-Chung Huang, Huang-Siang Lan, C. W. Liu, Y.-H. Huang*, Bigchoug Hung*, K.-T. Chan*, Michael Huang*, and M.-T. Yang*
National Taiwan University, Taiwan
*MediaTek Inc., Taiwan

Impact of via-last through-silicon via (TSV) on 28nm node devices is investigated. The stress field of TSV is affected by the back-end-of-line (BEOL) dielectrics. The absolute value of radial stress is different from that of tangential stress on silicon, which leads to the asymmetric keep-out zone (KOZ). The physics behind the asymmetry is also described. A modified KOZ model considering the asymmetric stress field is proposed and verified by experiment data.

4:40 P.M.
T11-3 Electrical Testing Structure for Stacking Error Measurement in 3D Integration

Shih-Wei Lee, Shu-Chiao Kuo, and Kuan-Neng Chen
National Chiao Tung University, Taiwan

A novel electrical test structure is proposed to inspect the stacking fault in 3D integration. This approach is one nondestructive analysis of the misalignment investigation. In order to determine the misalignment of wafer/chip stacking, the metal line pattern is designed to detect the direction and quantity of stacking fault. Testing circuit diagram is proposed and simulated for efficient measurement. In addition, different types of stacking fault including translation, rotation, and run out are discussed and formulated.

5:00 P.M. Break

Joint Panel Discussion
Tuesday, April 26, 5:00 P.M. ~ 6:30 P.M.
Ballroom B

Panel Topic: **IOT: Evolution or Revolution? Industry Realities and Market Implications**

Moderator: **Raj Jammy**, Carl Zeiss, USA

IoT will essentially change everything we do today requiring technology changes - conversely, we will need to apply existing technologies to build some part of IoT as we see it today and grow it further. Changes in processors, memory, connectivity, power management, power supply (batteries or harvesting), security, etc. are contemplated. With these changes the vast potential of IoT could be realized. But is the industry ready to change tried and tested devices and infrastructure so rapidly - equivalent to a revolution. Or, will the adoption be slower, building on existing technologies, more like an evolution? Where do the experts on the panel think this is headed?

Co-organizers :
Franz Dielacher, Infineon Technologies Austria AG, Austria
Shye-Jye Jou, National Chiao Tung University, Taiwan

Panelists:
Patrick Reynaert, KU Leuven, Belgium
Pangan Ting, Industrial Technology Research Institute, Taiwan
Franz Dielacher, Infineon Technologies Austria AG, Austria
Yuan-Kuang Tu, Chunghwa Telecom Co., Ltd., Taiwan
Clement Lin, NEXCOM International Co., Ltd., Taiwan
Allan Yang, Advantech Co., Ltd., Taiwan

Session J4: Joint Plenary Session
Wednesday, April 27, 8:30 A.M. ~ 10:10 A.M.
Ballroom B
Chair: Wu-Tung Cheng, Mentor Graphics, USA

8:30 A.M.
J4-1 For Your Eyes Only? UAV and DJI
Zexiang Li
Hong Kong University of Science and Technology, Hong Kong

James Bond and the costly U---2s were needed to locate military targets in the Cold War. Later, UAVs were introduced for reconnaissance operations. Although “they save lives”, these UAVs were still too expensive and inaccessible to civilians. As of 2012, USAF deployed about 7500 UAVs.Starting in the 1990’s, research programs were introduced in the robotics community to develop and miniaturize UAV technology for civilian use. Based on this work, a final---year project was done in 2005 at HKUST, aiming to develop a helicopter flight controller. Later, Frank Wang went on to found a UAV company by the name of DJI and introduced the Phantom family, a series of ready---to---fly UAVs equipped with gimbal---stabilized cameras.Combining consumer---level price and good user experience, the Phantom quickly became a popular device among hobbyists, filmmakers, and consumers. A new market for easy---to---fly aerial robotics that anyone could use emerged. Today the Phantoms are widely utilized in aerial photography/filmmaking, agriculture, sports, and infrastructure inspection and more. The drone market in 2015 is expected to break the one million unit benchmark.

9:20 A.M.
J4-2 Taiwan 4G Progress and 5G Evolution
Mu-Piao Shih
Chunghwa Telecom Co., Ltd., Taiwan

* Global and Taiwan 4G Update
* Opportunities and Challenges
* Evolution from 4G to 5G
* Concluding Remarks

10:10 A.M. Break

Session T12: Special Session - Green Electronics
Wednesday, April 27, 10:20 A.M. ~ 12:25 P.M.
Ballroom B
Chair: Wilman Tsai, TSMC, USA

10:20 A.M.

T12-1 On the Continuation of IC Innovation Against All Odds (Invited)

Paolo A. Gargini
ITRS, USA

The semiconductor industry is one, if not the only one, industry that began with a roadmap. Dr. Gordon Moore introduced the concept of roadmap for Integrated Circuit in 1965 and further refined it in 1975. His prediction of the doubling in the number of transistors every 2 years has applied for the past 40 years and will continue to hold for the next decade. A formal and detailed National technology Roadmap for Semiconductors (NTRS) was initiated in the US in 1992 and expanded to international participation (ITRS) in 1998. This roadmap was built as a “bottom up” approach characterized by showing how the increasing performance of transistors and Integrated Circuit enabled continuous improvements in system performance. The development of Foundry Companies and Design (Fabless) Companies in the late 90s led to the introduction of smart phones, tablets, set top boxes and many other innovative products in the past 10 years.

The net result of this industry evolution consisted in the fact that system houses had now become the drivers of the requirements for most of the leading ICs. For this reason the roadmap process has evolved in the past 2 years into ITRS 2.0 in which system requirements are highlighted as driver of the IC industry. The latest results and predictions will be presented.

10:55 A.M.

T12-2 Review of Negative Capacitance Transistors (Invited)

Sayeef Salahuddin
University of California, Berkeley, USA

Phase transition materials have long been investigated for fundamental physics and also for potential application in electronics. In this presentation, I shall discuss how a controlled phase transition can lead to fundamentally new switching devices that has significantly less energy dissipation compared to the state of the art. In particular, I shall talk about the state of negative capacitance that can be achieved in certain material systems with stored energy of phase transition. Our recent experiments with ferroelectric materials have shown that such a state of negative capacitance can actually be achieved. I shall also describe our very recent results where such negative capacitance, when combined with conventional transistors, lead to effects that was long believed to be impossible.

1:30 A.M.

T12-3 Atomistic Simulation of Gate-All-Around GaSb/InAs Nanowire TFETs Using a Fast Full-Band Mode-Space NEGF Model (Invited)

Aryan Afzalian, Matthias Passlack, and Yee-Chia Yeo*
TSMC, Belgium and *Taiwan

III-V gate-all-around (GAA) nanowire (NW) heterojunction TFETs have the potential to replace conventional Si MOSFET technologies as a low power sub-10 nm technology option. Accurate modeling of III-V nanowires with technology relevant dimensions requires computationally very expensive full-band quantum transport studies such as atomistic tight binding simulations within the NEGF framework.
We have recently demonstrated more than 100× reduction in simulation time using a tight binding mode-space (MS) approach. In this talk, we will review the recent advance in the field and present a comprehensive MS atomistic simulation assessment of the potential of InAs/GaSb GAA NW n and p-TFETs for future CMOS generations.

12:05 P.M.

T12-4 Band Structure Engineered Germanium-Tin (GeSn) p-channel Tunnel Transistors (Late News Paper)

Rahul Pandey*, Ramkrishna Ghosh*, and Suman Datta*,**
*The Pennsylvania State University, USA
**University of Notre Dame, USA

In this work, we perform a detailed materials and device design evaluation for p-channel homo-junction and hetero-junction Tunnel FETs in Ge and GeSn material system. We start with atomistic level materials simulation using first principles density functional theory (DFT) and extend it to device level TCAD simulation. We show clearly the impact of tuning Sn composition to engineer the band structure and control the relative contribution of the direct and phonon assisted indirect band-to-band tunneling to design and demonstrate p-channel Tunnel FET in the Group IV system that are competitive with their III-V compound semiconductor counterparts.

12:25 P.M. Lunch

Session T13: RRAM II
Wednesday, April 27, 10:20 A.M. ~ 12:15 P.M.
Ballroom C
Chair: Tuo-Hung Hou, National Chiao Tung University, Taiwan

10:20 A.M.
T13-1 Doping Technology for RRAM - Opportunities and Challenges (Invited)
Blanka Magyari-Köpe, Dan Duncan, Liang Zhao, and Yoshio Nishi
Stanford University, USA

Resistive random-access memory (RRAM), one of the most promising candidates for next generation non-volatile memory technology, nowadays still faces a series of challenges including switching-parameter variability, cycling endurance, and data retention. In order to cope with these challenges, ionic doping techniques have been widely explored to achieve better performance and reliability, through fine-tuning the switching material properties. The major factors that potentially affect the forming characteristics of doped transition metal oxides were systematically evaluated with density functional theory (DFT) calculations in conjunction with experimental observations to address the opportunities and challenges in achieving tunable RRAM characteristics.

10:55 A.M.
T13-2 Effect of Ti Buffer Layer on HfO_x-Based Bipolar and Complementary Resistive Switching for Future Memory Applications
Sk. Ziaur Rahaman, Yu-De Lin, Pei-Yi Gu, Heng-Yuan Lee, Yu-Sheng Chen, Pan-Shiu Chen*, Kan-Hsueh Tsai, Wei-Su Chen, Chien-Hua Hsu, Po-Tsung Tu, Frederick T. Chen, Ming-Jinn Tsai, Tzu-Kun Ku, and Pei-Hua Wang
Industrial Technology Research Institute, Taiwan
*MingShin University of Science and Technology, Taiwan

This paper investigates the Ti thickness modulation based simple strategy to regulate the oxygen vacancy concentrT13-ation in the HfO_x film and implemented to realize the resistive switching properties. Accordingly, we demonstrated a way to control the forming voltage, decrease the operation current to sub-μA level, controllable BRS/CRS and to bypass the self-CRS phenomena in Ti/HfO_x based 1T1R RRAM devices for future memory applications.

11:15 A.M.
T13-3 Low power/self-compliance of resistive switching elements modified with a conduction Ta-oxide layer through low temperature plasma oxidization of Ta thin film
Yu-Sheng Chen, Heng-Yuan Lee, Pang-Shiu Chen*, Y. D. Lin, Kan-Hsueh Tsai, C.H. Hsu, W. S. Chen, Ming-Jinn Tsai, T. K. Ku, and P. H. Wang
Industrial Technology Research Institute, Taiwan
*MingShin University of Science and Technology, Taiwan

A Ta ultra-thin metal layer was treated by O_2 plasma at low temperature to form TaO_x, which severs as a resistive element or internal resistor. The low current operated Ta/TaO_x/HfO_x and Ta/TaO_x/AlO_x devices exhibit self-compliance, good LRS nonlinearity (>40), robust retention at 85 °C, and enough endurance (>1000). A plausible mechanism is proposed. The low temperature plasma oxidation of Ta layer is demonstrated an potential process for vertical RRAM with self-compliance and low current operation of 5 μA.

11:35 A.M.

T13-4 Comprehensive Study of Intrinsic Unipolar SiO_x-Based ReRAM Characteristics in AC Frequency Response and Low Voltage (< 2V) Operation

Ying-Chen Chen, Yao-Feng Chang, Burt Fowler, Fei Zhou, Xiaohan Wu, Cheng-Chih Hsieh, Heng-Lu Chang, Chih-Hung Pan*, Min-Chen Chen*, Kuan-Chang Chang*, Tsung-Ming Tsai*, Ting-Chang Chang*, and Jack C. Lee
The University of Texas at Austin, USA
*National Sun Yat-Sen University , Taiwan

Intrinsic unipolar SiO_x-based Resistive-RAM (ReRAM) characteristics have been investigated. The cross-bar MIM structures have been examined under AC frequency response, by varying device area, temperature and current states. The results provide additional insights into the hopping/switching mechanisms. For the first time, by using SiO_x/HfO_x stacking engineering, we have developed a low-voltage operation (< 2V) for SiO_x-based ReRAM. The SiO_x/HfO_x stacking optimization not only maintains the RS behaviors even in air environment without any programming window degradation, but also further reduces the switching voltage below 2V.

11:55 A.M.

T13-5 A New Manufacturing Method of CMOS Logic Compatible 1T-CRRAM

Hung-Yu Chen, Hsien-Hao Chen, Yun-Feng Kao, Ping-Yu Chen, Ya-Chin King, and Chrong Jung Lin
National Tsing-Hua University, Taiwan

This study proposed a new manufacturing method for improving the fabrication yield of CRRAM in advanced 90nm CMOS logic process. The original CMOS compatible CRRAM is proposed to fabricate by the thickness and size control of contact etch process. Due to the variation of contact hole etch on different ILD topographies, the remained RRAM’s TMO could result in uniformity and yield problems of memory arrays. In order to decline the production variation, a new refilling Contact RRAM process is firstly proposed and demonstrated in this paper.

12:15 P.M. Lunch

TSA Short Course 1: Advanced Process Technology (ALD/ ALE)
Wednesday, April 27, 1:30 P.M. ~ 4:50 P.M.
Ballroom A
Course Organizer and Chair: Robert D. Clark, TEL Technology Center, America, LLC, USA

1:30 P.M.
Atomic Layer Deposition for Nanoelectronic Devices
Instructor: Paul C. McIntyre, Stanford University, USA

I. Atomic Layer Deposition (ALD) Chemistry Overview
- precursor selection
- kinetics: initiation and steady-state
- film purity
- plasma enhanced ALD
- characterization of ALD process and films

II. ALD of metal oxide dielectrics
- gate dielectrics on silicon and germanium
- compound semiconductor channels
- graphene and 2D materials
- capacitor dielectrics, initiation on metal surfaces

III. ALD of metal nitrides

IV. ALD of metals
- reaction mechanisms
- role of oxidant
- incubation and morphology evolution

V. Atomic layer epitaxy revisited

3:00 P.M. Break

3:20 P.M.

Atomic Layer Etching to Enable 7nm Technology Node and Beyond

Instructor: Alok Ranjan, TEL Technology Center, America, LLC, USA

With shrinking critical dimensions, dry etch faces more and more challenges. Minimizing each of aspect ratio dependent etching (ARDE), bowing, undercut, selectivity, and within die uniformly across a wafer are met by trading off one requirement against another. The problem of trade-offs is especially critical for 10nm and beyond technology. At the root of the problem is that roles radical flux, ion flux and ion energy play may be both good and bad. Increasing one parameter helps meeting one requirement but hinders meeting the other. Self-limiting processes like atomic layer etching (ALE) promise a way to escape the problem of balancing trade-offs. ALE [1] was realized in the mid-1990s but the industrial implementation did not occur due to inherent slowness and precision loss from improper balance of self-limiting passivation and its removal processes. In recent years interest in ALE has revived and strides have been made by etch equipment manufacturers primarily through temporal, spatial or combination of these two pulsing approaches. Moderate success has been reported with some of the trade-offs purported to be managed. Difficulty meeting requirements is due to the inability of plasma technologies to control ion energy at low and precise values.

In this short course, approaches to achieve very low plasma potential, high radical flux and high bombardment flux will be discussed. We demonstrate that ALE can achieve zero ARDE and infinite selectivity. Experimental results will highlight that careful consideration of surface process physics is required to achieve ALE and not simply “slow etching”. Without profile control, ALE is not useful. Profile control will be shown to rely on careful management of the ion energies and angles. ALE using three approaches for radical adsorption (1. Chemisorption, 2. Polymer deposition, and 3. Surface modification) and desorption using 2 approaches (1. Ion bombardment, 2. Substrate heating) will be addressed with insights to solve critical problems associated with Si (Gate, Fin), SiO_2 (Self-Aligned Contact), SiN (Gate Spacer, SIT spacer) etch.

[1] S. Athavale and D. J. Economou, J. Vac. Sci. Technol. B, 14, 3702 (1996).

[2] M. Wang and M. J. Kushner, J. Appl. Phys., 107, 023308 (2010)

TSA Short Course 2: Power Electronics
Wednesday, April 27, 1:30 P.M. ~ 4:50 P.M.
Ballroom B
Course Organizer: Ming-Jinn Tsai, Industrial Technology Research Institute, Taiwan
Chair: Chih-Fang Huang, National Tsing Hua University, Taiwan

1:30 P.M.
High Voltage Power Device Technologies : Si and Wide Bandgap Semiconductors
Instructor: T. Paul Chow, Rensselaer Polytechnic Institute, USA

> The physics, design and fabrication technologies of discrete and integrable semiconductor devices capable of blocking high voltages and conducting high currents are succinctly presented. Devices include pin, Schottky and advanced rectifiers, power MOSFETs and bipolar transistors, and thyristors. Performance demonstrations and potentials of emerging SiC and GaN devices are reviewed and compared with silicon counterparts.